REMARKS

Claims 15-17 and 20 are canceled herein. Claims 1, 18, 21 and 22 are amended herein. Claims 1-14 and 18, 19, 21 and 22 remain pending in the application.

The Applicant respectfully requests the Examiner to reconsider his earlier rejections in light of the following remarks. No new issues are raised nor is further search required as a result of the changes made herein. Entry of the Amendment is respectfully requested.

In the Drawings

Fig. 2 was objected because Applicant's proposed drawing change to Fig. 2 allegedly adds confusion with respect to what the applicant considers "Vo".

The Applicant made the drawing change as required by the previous Office Action. Applicant added "Vo" to the source voltage to correspond to the specification at page 4, line 6 of the specification.

Fig. 4 was objected because it allegedly does not show "Vo", which is described on page 4, line 6 of the specification.

Fig. 4 is described in the specification at page 6, lines 15-24, not at page 4, line 6 as alleged by the Examiner. Page 4, line 6 of the specification refers to Fig. 2.

The Applicant respectfully requests withdrawal of the objection to Figures 2 and 4.

Specification informality

The disclosure was objected to for an alleged informality. In particular, the Examiner alleges that switch MC, described at page 7, line 18 of the disclosure should be labeled switch MS.

A reading of the entire paragraph, page 7, lines 17-22, shows the labels of the referenced switches is correct. The Applicant is describing using the mirror path to equalize the current level on both sides of the current source switch MC. Withdrawal of the objection is respectfully requested.

Section 112 rejection of Claims 15-17 and 20-22

Claims 15-17 and 20-22 were rejected under 35 USC 112, second paragraph. The Applicant respectfully traverses the rejection.

Claim 15-17 and 20

Claims 15-17 and 20 are deleted herein, making the rejection of those claims now moot.

Claims 21 and 22

The Office Action alleges that the language "continuously receives said current flowing from said current source" is still misleading from claims 21 and 22. The Applicant respectfully disagrees.

A reading of the entire claim language indicates the limitation reads "substantially continuously receives said current flowing from said current source". The mirror path diverts the charge injection to ground when the switch at the current source is initially opened. Therefore, the load substantially continuously receives current since the charge injection only exists for a very short time when current switch initially allows current to flow to a load.

All the claims are in full conformance with 35 USC 112, and the Applicant requests the rejections be withdrawn.

Claims 1-5, 8-10 and 12-22 over Ravon

In the Office Action, claims 1-5, 8-10, 12 and 18-22 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by US Patent No. 6,137,275 to Ravon ("Ravon"), and claims 13-17 are rejected as obvious over Ravon. The Applicant respectfully traverses the rejection as follows.

Claims 15-17 and 20 are canceled herein, making the rejection of those claims moot.

Claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22 recite, *inter alia,* reduction of charge injection.

Ravon appears to teach a system for providing a regulated voltage meant to supply a load (Ravon, Abstract). A current source providing the maximum current likely to be surged by the load, and a device for receiving the constant current and regulating the load supply voltage (Ravon, Abstract). A

source 11 provides a constant voltage to a load, within a maximum current value that the load is likely to consume (Ravon, col. 3, lines 35-43). A regulating device 10 eliminates transients of the voltage supply to a load (Ravon, col. 3, lines 24-34). The regulating device includes a MOS power transistor M1, a MOS transistor M2, a transistor bias control circuit 13, and a comparator 14 (Ravon, Fig. 2; col. 3, line 49-col. 5, line 18). Transistor M2 controls the flow of current from the current source to ground (Ravon, Fig. 2). Transistor M1 controls the flow of current from the current source to the load (Ravon, Fig. 2).

Ravon's system is designed to supply a regulated voltage, at varying currents but within a maximum surge current (Ravon, col. 3, lines 35-44). The duel paths within Ravon's item 10 operate to limit transient variations of voltage Vout supplying a load, e.g., a microprocessor (Ravon, col. 3, lines 24-27). Elimination of voltage transients is NOT reduction of charge injection, as claimed by claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22.

The Office Action alleges Harton's duel paths operate to reduce charge injection (Office Action, pages 5, 6, 15 and 16). The Applicant respectfully disagrees.

Charge injection relates to the current spike that occurs most frequently during a switch state of either a MOS transistor switch or, more seriously, when a current source enters its saturation from a triod state, minority carriers from the inversion layer of the current source may be injected into the load. Ravon teaches the purpose of MOS transistor M2 is to absorb excess current during periods when the load only requires a low supply current. Ravon's current source is not taught as even being capacitive, and producing current spikes during switching. Ravon's **load** is creating the current fluctuations. Loads do not create charge injection. Reducing excess current during periods when the load only requires a low supply current (col. 3, lines 59-62) is **NOT** charge injection, as claimed by claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22.

Claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22 recite, *inter alia,* a pull-down mirror path in parallel with a transistor switch operating to equalize the current level produced by a current source.

Ravon fails to even mention the duel paths operating to equalize the current level produced by a current source. A method for two paths to equalize the current level produced by a current source is, e.g., each path having a matched impedance. Since current is a function of impedance, if each path has equal impedance, the current level produced by the current source would remain constant no matter which path is conducting current. Ravon fails to teach a pull-down mirror path in parallel with a transistor switch operating to equalize the current level produced by a current source, as claimed by claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22.

Accordingly, for at least all the above reasons, claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 6, 7 and 11 over Ravon in view of AAPA

In the Office Action, claims 6, 7 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Ravon in view of Applicant's Admitted Prior Art Fig. 3 (AAPA). The Applicant respectfully traverses the rejection as follows.

Claims 6, 7 and 11 are dependent on claim 1, and are allowable for at least the same reasons as claim 1 is allowable.

Claims 6, 7 and 11 of the present application recite, *inter alia,* reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

As discussed above, Ravon fails to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

The Office Action correctly acknowledged that Ravon fails to teach a serial combination of transistors. The Office Action relies on AAPA to make up for the deficiencies in Ravon to arrive at the claimed invention. The Applicant respectfully disagrees.

AAPA teaches an unsatisfactory circuit for reducing charge injection which uses a serial combination of transistors forming a compensating switch (AAPA, Fig. 3). AAPA fails to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize the current level produced by a current source, as claimed by claims 6, 7 and 11.

AAPA and Ravon fail to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize the current level produced by a current source, as claimed by claims 6, 7 and 11.

Accordingly, for at least all the above reasons, claims 6, 7 and 11 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-5, 8-10 and 12-20 in view of Harston

In the Office Action, claims 1-5, 8-10, 12-14, 18 and 19 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over US Patent No. 5,343,196 to Harston ("Harston"). The Applicant respectfully traverses the rejection as follows.

Claims 15-17 and 20 are canceled herein, making the rejection of those claims moot.

Claims 1-5, 8-10, 12-14, 18 and 19 of the present application recite, *inter alia,* reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

Harston teaches a method of reducing the amount of current switched to a reference line so as to reduce the overall power consumption of a digital to analog converter (DAC). To achieve this, three transistors are employed. One MOS transistor acts as a current source. The two other transistors act alternatively to direct current to either the load or ground (Harston, col. 1, line 41-42). The current directed to ground performs no useful purpose (Harston, col. 1, lines20-23).

Harston uses two transistors in a duel path to change states of a DAC, i.e., when it is on and off. Harston's current is NOT directed to ground in

one of the paths to reduce charge injection, as claimed by claims 1-5, 8-10, 12-14, 18 and 19.

Claims 1-5, 8-10, 12-14, 18 and 19 recite, *inter alia*, a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

Harston is unconcerned with equalizing the current level produced by a current source. Harston simply changes the state of a DAC as either receiving current from a source or not receiving current from a source.

Accordingly, for at least all the above reasons, claims 1-5, 8-10, 12-14, 18 and 19 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 6, 7 and 11 over Harston in view of AAPA

In the Office Action, claims 6, 7 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Harston in view of AAPA. The Applicant respectfully traverses the rejection as follows.

Claims 6, 7 and 11 are dependent on claim 1, and are allowable for at least the same reasons as claim 1 is allowable.

Claims 6, 7 and 11 of the present application recite, *inter alia,* reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

As discussed above, Harston fails to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

As discussed above, AAPA fails to teach a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load.

Harston and AAPA fails to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source, as claimed by claims 6, 7 and 11.

Accordingly, for at least all the above reasons, claims 6, 7 and 11 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Response to Arguments

The Examiner appears to maintain that the purpose of the cited references is to reduce the amount of current to a load, which equates to the claimed charge injection. The Applicant respectfully disagrees.

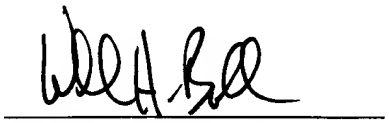
The Applicant's invention redirects a current spike produced by a capacitive current source to ground. Current spikes produced by a capacitive current source are released at the time the current source is switched on. Neither of the cited references recite a reduction of charge injection. The references reduce current, **not** charge injection as in the present invention. The Examiner is reading features into the references that simply are not taught by the cited prior art.

Conclusion

For at least all the above reasons, claims 1-14, 18, 19, 21 and 22 are patentable over the prior art of record.

All rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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Version with Markings to Show Changes Made

1. (Three Times Amended) A current source switching circuit with reduced charge injection, comprising:

a current source;

a transistor switch;

a pull-down mirror path in parallel with said transistor switch operating to equalize a current level produced by said current source; and

a first load;

wherein said transistor switch and said pull-down mirror path operate to substantially continuously reduce said charge injection flowing to said first load.

18. (Three Times Amended) A method of reducing charge injection from a current source through a current switch into a load, said method comprising:

providing a pull-down mirror path in parallel with said current switch, said pull-down mirror path and said current switch operating to equalize a current level produced by said current source;

turning a switch in said pull-down mirror path on when said current switch is turned off; and

turning said switch in said pull-down mirror path off when said current switch is turned on;

wherein said current switch and said pull-down mirror path operate substantially continuously to reduce said charge injection flowing to said load.

21. (Twice Amended) A method of switching a current source out from a load, said method comprising:

opening a transistor switch connecting said current source to said load; and

substantially simultaneously with said step of opening, closing a switch to a pull-down mirror path in parallel with said transistor switch so that current from said current source flows through said pull-down mirror path, said pull-down mirror path and said transistor switch operating to equalize a current level produced by said current source;

wherein said load substantially continuously receives said current flowing from said current source to reduce charge injection from said current source to said load when said transistor switch is opened.

22. (Twice Amended) Apparatus for switching a current source out from a load, comprising:

means for opening a transistor switch connecting said current source to said load; and

means for closing a switch to a pull-down mirror path in parallel with said transistor switch at substantially simultaneously a same time as said means for opening opens said transistor switch so that current from said current source flows through said pull-down mirror path, said pull-down mirror path and said transistor switch operating to equalize a current level produced by said current source;

wherein said load substantially continuously receives said current flowing from said current source and charge injection from said current source to said load when said transistor switch is opened is reduced.